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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,495	08/31/2000	Salman Akram	3847US (98-541)	3659

7590 11/29/2006

EXAMINER
PAREKH, NITIN

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ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/652,495	AKRAM, SALMAN	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-41 and 43-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-41 and 43-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12-21-05,5-30-06,6-16-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5-9, 19, 21, 22, 30-35, 43, 44 and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US Pat. 5258648) in view of Horiuchi et al. (US Pat. 6297553).

Regarding claim 1-3, 5-9 and 19, Lin discloses a chip scale package (CSP)/flip chip composite package/flip chip carrier (FCC see 10 in Fig. 1-5) comprising:

- a semiconductor device/silicon chip (12 in Fig. 1) including an active surface having bond pads (14 in Fig. 1), the device being invertedly disposed on a first/top surface of an interposer substrate (22 in Fig. 1-5)
- the interposer substrate comprising a semiconductor material such as silicon (Col. 6, lines 30-40) having substantially the same coefficient of thermal expansion (CTE) as that of the device/chip, the device/chip and the interposer substrate (12 and 22 respectively

in Fig. 1 and 3) having respective first and second thicknesses being substantially the same

- the interposer substrate having electrically conductive traces (26 in Fig. 1) on a first surface, being disposed adjacent the active surface of the device and the substrate including a plurality of electrically conductive/filled vias (ECV) on respective contact areas extending directly there-through (24 in Fig. 4; Col. 4, lines 52-65), the electrically conductive filled vias/material having one end being in electrical communication with/bonded to the conductive traces/contact areas and corresponding bond pads (Fig. 1-4) of the device, and
- electrically conductive solder balls/bumps (32 in Fig. 4; Col. 5, line 23) protruding from a second surface, the second surface being opposite to the first surface and the bumps being in electrical communication with respective electrically conductive vias

(Fig. 1-6; Col. 3, line 55- Col. 8, line 65).

Lin further discloses:

- the substrate having conductive traces in communication with the ECV, the traces being carried on/routed on the opposite surface/bottom surface extending in lateral directions from an end/second end of the ECV of the plurality of the conductive vias (see traces 43/44 with respect to the solder balls/vias in Fig. 6; Col. 8, line 55-60; Col. 7, line 35-55) to provide the desired routing for the vias and power/ground connections for the terminals/solder balls (Col. 6-8), and
- the electrically conductive solder balls/bumps (32 in Fig. 4; see Col. 5, lines 5-14; Col. 8, lines 58-60) protruding from the substrate opposite the semiconductor device at the bottom surface of the interposer substrate, being in communication

with respective ECV, and further being offset from the ECV and located at an opposite end of the conductive trace from the ECV.

Lin fails to teach the ECV comprising solder.

Horiuchi et al. teach a CSP having an interposer having conventional ECV comprising solder (32 in Fig. 2; Col. 5, lines 33-35; Col. 4 and 5).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the ECV comprising solder as taught by Horiuchi et al. so that the interconnect reliability can be improved and stress can be reduced in Lin's package.

Regarding claims 21, 22 and 30-35, Lin and Horiuchi et al. teach the entire claimed structure as applied to claim 1 above.

Regarding claims 43, 44 and 50-52, Lin and Horiuchi et al. teach the entire claimed structure as applied to claim 1 above.

3. Claims 11-14, 20, 23-25, 37-41 and 45-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Lin (US Pat. 5258648) and Horiuchi et al. (US Pat. 6297553) as applied to claims 1, 21 and 43 above, and further in view of Gnadinger (US Pat. 5229647).

Regarding claims 11-14, Lin and Horiuchi et al. teach substantially the entire claimed structure as applied to claim 1 above, except the second surface of the substrate being partially coated or substantially extended over with an insulating material.

Gnadinger teaches the multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, the insulating layer extending substantially over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second surface of the substrate being partially coated or substantially extending over with an insulating material as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Horiuchi et al. and Lin's package.

Regarding claim 20, Lin and Horiuchi et al. teach substantially the entire claimed structure as applied to claim 1 above, except forming a diffusion region comprising a bond pad and via material.

Gnadinger teaches the multichip package where a diffusion region is formed comprising via, bond pad and their material, the region securing the device to the substrate (23 in Fig. 4; Col. 4, line 23).

It would have been obvious to one of ordinary skill in the art at the time invention was made incorporate a diffusion region between the bond pad and via, the region securing the device to the substrate as taught by Gnadinger so that the metallurgical bonding and electrical performance of the device can be improved in Horiuchi et al. and Lin's package.

Regarding claims 23-25, Lin, Horiuchi et al. and Gnadinger teach substantially the entire claimed structure as applied to claims 1, 21 and 20 above.

Regarding claims 37-41, Lin, Horiuchi et al. and Gnadinger teach substantially the entire claimed structure as applied to claims 1, 21 and 11-14 above.

Regarding claims 45-49, Lin, Horiuchi et al. and Gnadinger teach substantially the entire claimed structure as applied to claims 1, 43 and 11-14 above.

4. Claims 10, 15, 18, 26, 27 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US Pat. 5258648) and Horiuchi et al. (US Pat. 6297553) as applied to claims 1 and 21 above, and further in view of Kim et al. (US Pat. 6004867)

Regarding claim 10, Lin and Horiuchi et al. teach substantially the entire claimed structure as applied to claim 1 above, except a first thickness of the semiconductor device being greater than that of the semiconductor substrate.

Kim et al. teach a CSP/FCC wherein a first thickness of the semiconductor device/chip (110 in Fig. 2) is greater than that of the semiconductor substrate (120 in Fig. 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate first thickness of the semiconductor device being greater than that of the semiconductor substrate as taught by Kim et al. so that manufacturing yield and processing/cycle time can be improved in Horiuchi et al. and Lin et al's package.

Regarding claims 15 and 18, Lin and Horiuchi et al. teach substantially the entire claimed structure as applied to claim 1 above, except an intermediate layer being disposed between the device and the substrate adhering the device and the substrate and the conductive vias, conductive traces and corresponding bond pads being in communication through the intermediate layer.

Kim et al. teach the CSP/FCC comprising an intermediate/passivation layer (114 in Fig. 2; Col. 3, line-5) being disposed between the device and the substrate adhering the device and the substrate.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate intermediate layer being disposed between the device and the substrate adhering the device and the substrate and the conductive vias, conductive traces and corresponding bond pads being in communication through the intermediate layer as taught by Kim et al. so that the surface protection can be improved in Horiuchi et al. and Lin's package.

Regarding claims 26 and 27, Lin, Horiuchi et al. and Kim et al. teach substantially the entire claimed structure as applied to claims 1, 21, 15 and 18 above.

Regarding claim 36, Lin, Horiuchi et al. and Kim et al. teach substantially the entire claimed structure as applied to claims 1, 21 and 10 above.

5. Claims 16, 17, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US Pat. 5258648) and Horiuchi et al. (US Pat. 6297553) as

applied to claims 1, 15 and 21 above and further in view of Kim et al. (US Pat. 6004867) and Higgins, III (US Pat. 6294405).

Regarding claims 16 and 17, Lin, Horiuchi et al. and Kim et al. teach substantially the entire claimed structure as applied to claims 1 and 15 above, except the intermediate layer comprising an adhesive material or polyimide.

Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide, silicon oxide, etc. (Col. 2, line 65) to provide a protection and bonding/adhesion for the device in a CSP.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an intermediate layer comprising an adhesive material as taught by Higgins, III so that the passivation and surface protection can be improved in Horiuchi et al., Kim et al. and Lin's package.

Regarding claims 28 and 29, Lin, Horiuchi et al., Kim et al. and Higgins, III teach substantially the entire claimed structure as applied to claims 1, 21 and 15-17 above.

6. Claims 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Lin (US Pat. 5258648) and Horiuchi et al. (US Pat. 6297553) as applied to claim 43 above, and further in view of Tokuda et al. (US Pat. 5870289).

Regarding claims 53-55, Lin and Horiuchi et al. teach substantially the entire claimed structure as applied to claims 1 and 43 above, except an adhesive layer disposed adjacent the first surface of the substrate.

Tokuda et al. teach a chip/substrate structure having through-holes/vias wherein a conventional adhesive layer/polyimide (see 30 in Fig. 1) is disposed adjacent/on a first/top surface of a wiring substrate (20 in Fig. 1) such that the through-holes/vias extend through the adhesive layer to provide the desired electrical connection (see 40 in Fig. 1; Col. 10, line 30- Col. 11, line 10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the polyimide/adhesive layer being disposed adjacent the first surface of the substrate wherein one end of at least one end of the via extends through the adhesive layer as taught by Tokuda et al. so that the passivation/ surface protection for the substrate can be improved in Horiuchi et al. and Lin's package.

Response to Argument

7. Applicant's arguments with respect to claims 1-3, 5-41 and 43-55 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rich Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

11-21-06

NITIN PAREKH

PRIMARY EXAMINER

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